IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:
Bernstein, et al. Atty. Docket No.: BUR920010178US1

Serial No.: 10/023,235 Group Art Unit: 2128

Filed: December 17, 2001 Examiner: Saxena, Akash

For: SYSTEM AND METHOD FOR TARGET-BASED COMPACT MODELING

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' APPEAL BRIEF

Sirs:

Appellant respectfully appeals the final rejection of claims 1-3, 5-11, 13-22, and 24-42, in the Office Action dated June 28, 2007. A Notice of Appeal was timely filed on September 27, 2007.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, Armonk, New York, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-3, 5-11, 13-22, and 24-42, all the claims pending in the application and under appeal, stand rejected under 35 U.S.C. §112, first and second paragraphs. Claims 1-27 and 30-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al., (U.S. Patent No. 6,269,277), hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic, further in view of applicant's own admission. Claims 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission, further in view of Peng et al. (U.S. Patent No. 6, 028, 994), hereinafter referred to as Peng. All rejection so f all pending claims 1-3, 5-11, 13-22, and 24-42 are appealed.

IV. STATUS OF AMENDMENTS

On August 28, 2007 an amendment was filed under 37 C.F.R. §1.116. The Amendment included corrections to fix typographical errors in claims 5 and 13. An

Advisory Action dated September 12, 2007 indicated that, the Amendment filed on August 28, 2007 did not place the application in condition for allowance, and that the rejections of claims would remain. The Advisory Action further indicated, without explanation, that the amendments would not be entered. Thus, the Appellants anticipate filing an amendment under 37 C.F.R. §1.312 after allowance to ensure that the errors are corrected. The claims shown in the appendix are shown in their entered form prior to the August 28, 2007 Amendment.

V. SUMMARY OF CLAIMED SUBJECT MATTER

It should be noted that all paragraphs cited in the summary of the claimed subject matter below refer to the paragraph numbers as show in the Published Patent Application No. 2003/0114944A1.

A. One embodiment, as claimed in claim 1, is a simulator (see paragraphs [0004] and [0047] of the specification, which disclose that the computer model of the invention comprises physics-based subroutines used in numerical simulation codes and, more particularly, that the target model is a set of equations (typically embodied in a set of software sub-routines that are part of a circuit network simulation program). See also paragraph [0049] which further discloses a representative hardware environment for practicing the present invention).

One feature of the invention is a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein the computer model is generated based on a target model for the device and wherein the target model is created using a target performance parameter range for the performance attribute and is adapted to predict process and design variations of the device. Claim 1 defines this feature as follows: "a memory for storing a computer model of an integrated circuit comprising a

device that comprises an integrated circuit component and that has at least one performance attribute, wherein said computer model is generated based on a target model for said device and wherein said target model is created using a target performance parameter range for said performance attribute and is adapted to predict process and design variations of said device." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0049] identifies a representative hardware environment for practicing the invention that includes memory. Paragraph [0007] describes this feature as follows: "there is provided, according to one aspect of the invention, a computer model ... of a device that has a performance parameter." Paragraph [0017] provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0022] provides that with the invention ... a compact model (the target model) is created for a device such as a metal-oxide semiconductor field-effect transistor (MOSFET) that reflects the process performance targets that are to be achieved at the end of the process development cycle. Paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404 and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). ... If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

Another feature of the invention is a processor in communication with the memory and adapted to determine the target performance parameter range and to execute the computer model. Claim 1 defines this feature as follows: "a processor in

communication with said memory and adapted to determine said target performance parameter range and to execute said computer model." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0049] identifies a representative hardware environment for practicing the invention that includes a processor connected via a bus to memory. Paragraph [0033] sets out various ways by which the performance parameter ranges 404 for a device can be determined.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 1 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range constrained by two variables: the first variable being variations in the manufacturing process and the second variable being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by model curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear model curve 22 for a design and the least linear model curve 20 for a design. This represents the second bounded

range, as claimed. Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range based on design variations and the multiple first bounded ranges around each curve 20-22 based on process variations).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 1 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that thr target performance parameter range is expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between

the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20.

Another feature of the invention is that each of the different designs for the device is directed to a variation of a single design for the integrated circuit. Claim 1 defines this feature as follows: " wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the same performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 1 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] explains that different designs for a device can be used to achieve the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the

least linear curve 20 (i.e., the second bounded range, as claimed, is constrained by the two curves 20 and 22).

B. Another embodiment of the invention, as claimed in claim 9, is a computer-implemented method for designing a product having a device comprising an integrated circuit components, wherein said product is tolerant to variance in a given target performance parameter for a given performance attribute of said device (see Figure 4 and associated text).

One feature of the method is designing the product using a computer model that is based on a target model of the device, wherein the target model is created using a target performance parameter range for the performance attribute. Claim 9 defines this feature as follows: "designing said product using a computer model that is based on a target model of said device, wherein said target model is created using a target performance parameter range for said performance attribute." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0007] describes this feature as follows: "there is provided, according to one aspect of the invention, a computer model ... of a device that has a performance parameter." Paragraph [0017] provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0022] provides that with the invention ... a compact model (the target model) is created for a device such as a metal-oxide semiconductor field-effect transistor (MOSFET) that reflects the process performance targets that are to be achieved at the end of the process development cycle. Paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404

and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). ... If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 9 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by model curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., includes the second bounded range, as claimed, due to different device designs). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of

the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 9 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 9 defines this feature as follows: "wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 9 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can achieve the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

C. Another embodiment of the invention, as claimed in claim 14, is a method of developing a product comprising a device with a least one performance attribute, wherein said device comprises an integrated circuit component (see Figure 4 and the associated text).

One feature of the invention is developing device goals for the device, wherein the device goals are based on product goals. Claim 14 defines this feature as follows: "developing device goals for said device, wherein said device goals are based on product goals." This feature is described at various points in the specification and is illustrated in Figure 4.

Specifically, paragraph [0017] of the specification provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0030] further provides that: "Device goals are established in item 402 and are based, at least in part, upon the circuit goals developed in item 432. At this point, the device goals are merely conceptual objectives that the device should achieve, and do not represent a true model of the device."

Another feature of the invention is developing a target performance parameter range for the performance attribute based on the device goals. Claim 14 defines this feature as follows: "developing a target performance parameter range for said performance attribute based on said device goals." This feature is described at various points in the specification and illustrated in Figure 4. Specifically, paragraph [0030] describes this feature as follows: "From these goals, the target performance parameters 404 are developed." This is shown in Figure 4.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 14 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range constrained by two variables): the first variable being variations in the manufacturing process and the second variable being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by model curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., includes the second bounded range, as claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 14 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 14 defines this feature as follows: " wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final

design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 14 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two model curves 20 and 22).

Another feature of the invention is producing a target model of the device based on the device goals and the target performance parameter range, wherein the target model is adapted to predict process and design variations of the device. Claim 14 defines this feature as follows: "producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device." This feature is described at various points in the specification and is illustrated in Figure 4. Specifically, paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as

much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process.

Another feature of the invention is designing the product with the device based on the target model. Claim 14 defines this feature as follows: "designing said product with said device based on said target model." This feature is described at various points in the specification and is illustrated in Figure 4.

Specifically, paragraph [0017] of the specification provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0034] provides that once a target model is completed, it is then made available to circuit designers since the circuit design can not formally proceed without some type of compact model. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404 and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). ... If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

D. Another embodiment of the invention, as claimed in claim 19, is a method of designing a device with at least one performance attribute, wherein the device comprises an integrated circuit component (see Figure 4 and the associated text).

One feature of the invention is providing a target model for the device, wherein the target model is created based on a target performance parameter range for the performance attribute. Claim 19 defines this feature as follows: "providing a target model for said device, wherein said target model is created based on a target performance parameter range for said performance attribute." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 4.

Specifically, paragraph [0017] of the specification provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 19 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., includes the second bounded range, as

claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 19 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter

points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is wherein each of the multiple different designs is directed to a variation of a single design for the device. Claim 19 defines this feature as follows: "wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 19 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most

linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

Another feature of the invention is developing a design for the device based on the target model. Claim 19 defines this feature as follows: "developing a design for said device based on said target model." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0022] provides that at the beginning of a new process technology ..., a compact model (the target model) is created for a device. Paragraph [0034] provides that process development groups begin the cycle of refining the device design in item 408 and further provides that optionally the model is used to update device design in items 410 and 420.

Another feature of the invention is proposing a modification of the design, wherein the modification comprises one of adding a particular feature into the design and modifying the particular feature already in the design. Claim 19 defines this feature as follows: "proposing a modification of said design, wherein said modification comprises one of adding a particular feature into said design and modifying said particular feature already in said design." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0034] provides that "If the simulations indicate that the targets are not met, processing returns to item 408 where the device design is modified. In item 416, hardware experiments are used to produce and test new device designs."

Another feature of the invention is determining primary parameters for the particular feature. Claim 19 defines this feature as follows: "determining primary parameters for said particular feature." This feature is described at various points in the specification and is illustrated in Figure 5.

Specifically, paragraph [0038] provides that a goal of the invention is to allow designers to examine how potential changes in the design of a device (e.g., a transistor) will influence circuits. The invention achieves this goal by correlating physical feature changes with target performance parameter changes. Paragraph [0039] provides that

primary device parameters are performance characteristics that are directly related to a specified physical feature. If a potential modification of a device design is proposed, the invention calculates primary device parameters from such physical features.

Another feature of the invention is determining secondary parameters from the primary parameters. Claim 19 defines this feature as follows: "determining secondary parameters from said primary parameters." This feature is described at various points in the specification and illustrated in Figure 5.

Specifically, paragraph [0039] indicates that the invention provides a correlation between the primary parameters and secondary parameters. Paragraph [0041] further provides that the secondary parameter is calculated based on one or more primary parameters, while the primary parameters are directly calculated from the physical features of the device.

Another feature of the invention is balancing design choices related to the modification and, particularly, to the primary parameters and the secondary parameters in order to maintain device performance within the target performance parameter range. Claim 19 defines this feature as follows: "balancing design choices related to said modification and, particularly, to said primary parameters and said secondary parameters in order to maintain device performance within said target performance parameter range." This feature is described at various points in the specification and illustrated in Figure 5.

Specifically, paragraph [0044] provides that the invention allows the device designers to play "what if" scenarios on the device design. It further provides that the features shown in Figure 5 allow a number of features in the design to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain performance within the range of target performance parameters. Thus, if a certain change in the physical design of the device causes a secondary device parameter to exceed the performance parameters, the invention allows the designer to change a different physical feature to see whether the performance an be brought back in line with the target performance parameters.

E. Another embodiment of the invention, as claimed in claim 24, is a method of developing a product comprising a device with at least one performance attribute, wherein the device comprises an integrated circuit component (see Figure 4 and the associated text).

One feature of invention is developing device goals for the device, wherein the device goals are based on product goals. Claim 24 defines this feature as follows: "developing device goals for said device, wherein said device goals are based on product goals." This feature is described at various points in the specification and is illustrated in Figure 4.

Specifically, paragraph [0017] of the specification provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0030] further provides that: "Device goals are established in item 402 and are based, at least in part, upon the circuit goals developed in item 432. At this point, the device goals are merely conceptual objectives that the device should achieve, and do not represent a true model of the device."

Another feature of the invention is developing a target performance parameter range for the performance attribute based on the device goals. Claim 24 defines this feature as follows: "developing a target performance parameter range for said performance attribute based on said device goals." This feature is described at various points in the specification and illustrated in Figure 4. Specifically, paragraph [0030] describes this feature as follows: "From these goals, the target performance parameters 404 are developed." This is shown in Figure 4.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 24 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range, as claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 24 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 24 defines this feature as follows: " wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final

design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 24 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

Another feature of the invention is producing a target model of the device based on the device goals and the target performance parameter range, wherein the target model is adapted to predict process and design variations of the device. Claim 24 defines this feature as follows: "producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device." This feature is described at various points in the specification and is illustrated in Figure 4. Specifically, paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as

much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process.

Another feature of the invention is creating a computer model of the product, wherein the computer model of the product is based on the target model, and simulating the computer model of the product to determine whether the product goals have been met. Claim 24 defines this feature as follows: "creating a computer model of said product, wherein said computer model of said product is based on said target model; and, simulating said computer model of said product to determine whether said product goals have been met." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0017] of the specification provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0034] provides that once a target model is completed, it is then made available to circuit designers since the circuit design can not formally proceed without some type of compact model. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404 and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). ... If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

F. Another embodiment of the invention, as claimed in claim 36, is a program storage device readable by computer and tangibly embodying a model of an integrated circuit device that has at least one performance attribute, the model, executable by the computer (see paragraph [0049] as well as Figure 4 and the associated text).

One feature of the invention is a set of subroutines created using a target performance parameter range for the performance attribute, wherein the set of subroutines, when executed by the computer, predict process and design variations of the device. Claim 36 defines this feature as follows: "a set of subroutines created using a target performance parameter range for said performance attribute, wherein said set of subroutines, when executed by said computer, predict process and design variations of said device." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process. Paragraph [0047] further provides that the target model 406 is a set of equations (typically embodied in a set of software subroutines that are part of a circuit network simulation program) that includes some features that are new (associated with the next generation of technology) and some features that are old (associated with the current, or previous, generations of technology)."

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 36 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as

a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range, as claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 36 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same

performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 36 defines this feature as follows: "wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter

variations between the multiple different designs for the device. Claim 36 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

G. Another embodiment of the invention, as claimed in claim 40, is a program storage device readable by computer and tangibly embodying a set of instructions executable by said computer to perform an integrated circuit development method (see paragraph [0049] as well as Figure 4 and the associated text).

One feature of the invention is producing a target model of a device for a product using a target performance parameter range for a performance attribute of the integrated circuit device, wherein the device comprises an integrated circuit component and wherein the target model comprises a set of subroutines that are adapted to predict process and design variations of the device. Claim 40 defines this feature as follows: "producing a target model of a device for a product using a target performance parameter range for a performance attribute of said integrated circuit device, wherein said device comprises an integrated circuit component and wherein said target model comprises a set of subroutines that are adapted to predict process and design variations of said device." This feature is described at various points in the specification and is illustrated in Figure 4.

Specifically, paragraph [0007] describes this feature as follows: "there is provided, according to one aspect of the invention, a computer model ... of a device that has a performance parameter." Paragraph [0017] provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0022] provides that with the invention ... a compact model (the target model) is created for a device such as a metal-oxide semiconductor field-effect transistor (MOSFET) that reflects the process performance targets that are to be achieved at the end of the process development cycle. Paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive of both process and device design variations, and of the final nominal process. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404 and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). ... If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 40 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures

2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range, as claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 40 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same

performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 40 defines this feature as follows: "wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter

variations between the multiple different designs for the device. Claim 40 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

H. Another embodiment of the invention, as claimed in claim 42, a computer-implemented method of developing a product comprising a device with at least one performance attribute, wherein said device comprises an integrated circuit component (see Figure 4 and the associated text).

One feature of the invention is designing the product using a computer model that is based on a target model of the device, wherein the target model is created using the target performance parameter range for the performance attribute. Claim 42 defines this feature as follows: "designing said product using a computer model that is based on a target model of said device, wherein said target model is created using said a target performance parameter range for said performance attribute." This feature is described at various points in the specification and illustrated in Figure 4.

Specifically, paragraph [0007] describes this feature as follows: "there is provided, according to one aspect of the invention, a computer model ... of a device that has a performance parameter." Paragraph [0017] provides that "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or

the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. Paragraph [0022] provides that with the invention … a compact model (the target model) is created for a device such as a metal-oxide semiconductor field-effect transistor (MOSFET) that reflects the process performance targets that are to be achieved at the end of the process development cycle. Paragraph [0020] provides that in the invention, rather than specifying the performance parameter as a single point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables. The first variable is expected variations in the manufacturing process itself, and the second variable is the variation in device design." Paragraph [0034] provides that a target model of the device is created using the target performance parameters and the device goals in item 406. The target model is constructed with as much attention to accuracy as possible, given the available information, since it must be predictive. Paragraph [0034] provides that once a target model is completed, it is then made available to circuit designers since the circuit design can not formally proceed without some type of compact model. Paragraph [0035] provides that the circuit design process relies upon the target performance parameters 404 and the target model 406 to create a circuit model 434 for the chip. The circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438). … If the circuit goals have been met, the circuit is physically produced and tested 440 using the devices from item 420.

Another feature of the invention is that the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Claim 42 defines this feature as follows: "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, paragraph [0007] of the published patent application provides that the invention relates to modeling a device that has a performance parameter with bounded ranges: (1) a first bounded range has performance parameter variations within a single manufacturing process; and (2) a second bounded range has performance

parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] of the published patent application and illustrated in Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range, as claimed, due to design variations). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges, as claimed, due to process variations. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve a same performance point. Claim 42 defines this feature as follows: "wherein each of said first bounded ranges comprises a range of performance parameter

variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded based on variations in processing windows (e.g., temperature, pressure, etc.) that cannot be controlled with precision. These variations are designated by dashed lines 25, 27 which surround each of the design curves 20-22 in Figure 2. Thus, the dashed lines 25, 27 surrounding each of the design curves 2-22 represent the multiple first bounded ranges. Paragraph [0030] specifically provides that since "the designer must consider both manufacturing process variations and design variations, the range of performance parameters 30 includes the parameter points between the upper manufacturing process window 27 of curve 22 and the lower manufacturing process window 25 of curve 20 (i.e., it includes both the second bounded range and the multiple first bounded ranges around each curve 20-22).

Another feature of the invention is that each of the multiple different designs is directed to a variation of a single design for the device. Claim 42 defines this feature as follows: "wherein each of said multiple different designs is directed to a variation of a single design for said device." This feature is described at various points in the specification and illustrated in Figures 2-3 and Figure 5.

Specifically, paragraphs [0024]-[0025] recognize that designers can design devices that achieve the performance point in different manners, as represented by curves 20-22 of Figure 2. That is, each device may be designed based upon the same target model; however, because of individual design choices, cost consideration, etc., the final design of the devices was each slightly different, thus resulting in the different curves 20-22. Paragraph [0042] further provides that "The features shown in Figure 5 also allow a number features to be altered, thereby allowing balancing of different design choices to achieve some goal, yet maintain the devices performance within the range of target performance parameters."

Another feature of the invention is that the second bounded range is constrained by at least two of the multiple model curves so as to comprise performance parameter variations between the multiple different designs for the device. Claim 42 defines this feature as follows: "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." This feature is described at various points in the specification and illustrated in Figures 2-3.

Specifically, as discussed above, paragraph [0025] further explains that different designs for a device can be used, while still achieving the same performance point, as illustrated by curves 20-22 of Figure 2. That is, curves 20-22 represent different designs for a device that are based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., the second bounded range is constrained by the two curves 20 and 22).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review is whether claims 1-3, 5-11, 13-22 and 24-42 are based on a disclosure which is not enabling, whether claims 1-3, 5-11, 13-22 and 24-42 are indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention, whether claims 1-27 and 30-42 are unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission and whether claims 28-29 are unpatentable over Hershenson, in view of Krivokapic, further in view of applicant's own admission, further in view of Peng.

VII. ARGUMENT

A. The Rejection Based on

1. The Position in the Office Action

Claim Interpretation

Regarding Claim 1

The phrase "performance parameter" is understood as the current voltage switch- point of a transistor computer model in reference to claim and as understood from specification [0018].

The phrase "second bounded range" is a range representing the variation in the "performance parameter" due to variation in the design of device. In other words, second bounded range represents a range of current voltage switch points of a transistor computer model due to variations in designs of a transistor. For example variations in design of transistor is understood as change in length & width of transistor.

Regarding Claim 19

The "primary parameters" of a feature as disclosed in the specification ([0039]) are performance characteristics that are directly related to the specific physical feature. For example, in MOSFET designs, the overlap capacitance (C.sub.ov) is directly related to the length of the physical overlap of the gate material over the diffusion and extension (or lightly-doped drain) implants and the gate oxide thickness.

The "secondary parameters" of a feature, as disclosed in the specification ([0040]-[0041]) are calculated based on the one or more primary parameters. For example total gate capacitance.

Response to Applicant's Remarks for 35 U.S.C. §103

Claim(s) 1, 9, 14, 19, 24, 36, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hershenson, in view of Krivokapic.

Regarding Claims 1, 9, 14, 19, 24, 36, 40 and 42

(Argument 1) Applicant has argued, "Nowhere in Hershenson does it disclose a target performance parameter range".

(Response 1) Examiner respectfully disagrees. Please see Hershenson below. Hershenson Col.3 Line 67-Col.4 Line 39 - where the performance specifications for the integrated

circuit topologies are described as posynomial functions of the design parameters (i.e. target performances). The performance specifications are combined with user defined design objectives and constraints to form a geometric program. One embodiment reformulates geometric programs as convex optimization problems, i.e., the problem of minimizing a convex function subject to convex inequalities constraints and linear equality constraints;

Hershenson Col. 7 Lines 30-50 - where the optimization problem based on the performance posynomial is expressed as an inequality bounded by range "less than or equal to one."

Hershenson Col.21 Lines 44-58 - where the (target parameter) performance can be handled in ranges.

(Argument 2) Applicant has argued, "Nowhere in Krivokapic is a target performance parameter range disclosed."

(Response 2) Teachings of Hershenson are used to teach target performance parameter in broadest possible interpretation — see argument I above. (Argument 3) Applicant has argued, "Neither Krivokapic, nor Hershènson teach the limiting feature that the target performance range includes first bounded ranges each comprising range of performance parameter variations due to manufacturing process variations and each based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point." (Response 3) Examiner respectfully disagrees, as combined teachings of Hershenson and Krivokapic teach the above limitations. First, Hershenson teaches bounded range for the process variations (See response to argument 1). As for process variations based on a corresponding one of the multiple model curves for different designs of said device, Hershenson teaches various circuit topologies performing the same function but optimized for various performance points (Hershenson: at least Col.5 Lines 40 —Col.6 Lines 24). Applicant's interpretation of topology is noted, however, the broadest reasonable interpretation of the claim language "different designs" includes the examiner's interpretations. Applicant's argument that '~different design" should be interpreted as disclosed in [0025], referring to different technology is not

present in claim. Examiner maintains the broadest interpretations and presents Hershenson where 3 possible device models are presented based on the circuit design (Hershenson: Col.6 Lines 1-24). Further to address the newly added limitation that "multiple first bounded ranges" representing the process variation for the target performance parameter, are taught by at least by Krivokapic (Krivokapic: See Fig.I) where the separate parameters 103-1 07 are presented to the device simulator leading to bound ranges 110 and multiple curves 109.

(Argument 4) Applicant has argued, "Nor do they (Hershenson and Krivokapic) teach or suggest that the target performance parameter also include a second bound range that is constrained by at least two multiple model cunies".

(Response 4) As shown Hershenson teaches performance analysis for at least 3 models (Hershenson: Col.6 Lines 1-24), thereby meeting the limitation of the second bound ranges. Krivokapic also teaches the above limitation (Krivokapic: Col.8 Lines 50-63). Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Claim Objections

Claims 5 & 6 either have typographical error or depend from cancelled claim 4.

Claim l3 is objected to as word "range" is repeated twice in the end.

Claim 25 is objected to as the status of the claim indicates, "previously presented" however the claim is clearly amended.

Claim 34 is objected to as the status of the claim indicates, "Currently Amended" however the claim is clearly not amended.

Claim Rejections -35 USC §112, first paragraph

Claim 1-3, 5-11, 13-22, 24-42 are rejected under 35 U.S.C. 112, first paragraph, as being based on a disclosure which is not enabling. Claims disclose generating computer model based on a target model where the target model is created using the performance parameters — the disclosure lacks enablement for creating such a computer model effectively based on performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure.

Claim Rejections -35 USC §112, second paragraph

Claim 1-3, 5-11, 13-22, 24-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1-3, 5-11, 13-22, 24-42

Independent claims 1, 9, 14, 19, 24, 36 and 40 disclose limitation "first bound range" and "second bound range" for a "performance parameter". However no specific ranges are provided for this claim thereby failing to provide for the metes and bound for the ranges.

Claim Rejections -35 USC §103

Claims 1-27 & 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277hereafter) in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission.

Regarding Claim 1 (Updated)

HE'277 teaches a simulator (HE'277: Col.4 Lines 61-Col.5 Line 6) comprising:
a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component (HE'277: Col.6 Lines 58-62 — a transistor) and has at least one performance attribute (HE'277: Col.3 Line 67 — CoI.4 Line 5; Col. I Lines 10-15); wherein the said computer model is generated based on the target model for said device (HE'277: CoI.6 Lines 58-62) and wherein said target model is create using performance parameter ranges for the said performance attribute (HE'277: Col.5 Lines 40-46; Also see ranges in KR'527 Fig.1 Elements 103- 107). The transistor models are posynomial models, which are created (optimized) for one or more performance specifications (HE'277: Col.6 Lines 3-6). HE'277 further teaches, said target model is adapted to determine the said target performance parameter range of said device (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48; Also See KR'527 — Fig.1 element 109). HE'277 teaches a processor in communication with the said memory and adapted to execute said computer model (HE'277: Col.4 Lines 61-Col.5 Line 6; Col.6 Lines 58-67).

HE'277 teaches target performance parameter range comprises multiple first bounded range (due to process variation being modeled as inequalities - HE'277 — single variation as function f0 and multiple variations as l~ - Col.7 Line 1-59 Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41) and a second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-5 1) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches each of said first bounded range~ comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model cunies for different designs of said device that achieves a same performance point (HE'277:
Col.20 Lines 6-21, CoI.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.21 Lines 35-49) and; HE'277 teaches said second bounded range comprises performance parameters variations between designs for said design device (HE'277: Col.1I Lines 40-Col.12 Linel6) as variations in at least the Length and Width of the transistor.
HE'277 teaches each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is contrainted by these curves.
HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process where the performance parameter are current voltage switch point (See claim interpretation), although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes [nature of problem being solved] (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col,3 Lines 9- 55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, as is known in the art, numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to predictively examine possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 2 (Updated)

HE'277 teaches that multiple designs are directed to variations of a single design (HE'277: Col.I I Lines 40-Col.12 Linel6). For example changing the width (W) and lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.1, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 3

HE'277 does not explicitly teach performance parameter range is the same for a target model of said device and a final hardware design of said device as the (performance) parameters are used for manufacturing and modeling. HE'277 also does not teaches interaction between the actual manufacturing and model simulation.

KR'527 teaches that performance parameter range is the same for a target model of said device and a final hardware design of said device (KR'527: Fig.6a, ~ as the (performance) parameters are used for manufacturing and modeling.

KR'527 teaches in interaction between the actual manufacturing and model simulation (KR'527: Col.9-1I).

Regarding Claim 5-7 (Updated)

HE'277 teaches using multiple constraints where the constraints vary as defined in the simulation, further HE'277 teaches performing tradeoff optimization between various constraints graphically displayed as curves (HE'277: Col.6 Lines 3-24). KR'527 also teaches statistical Monte Carlo based inputs (as ranges) & range correction (KR'527: Fig.6b, Col.12 Lines 8-50). Plurality of performance points (range) are selected as various input parameter values from statistical distributions mentioned above. Multiple first bound ranges can be seen in (KR'527: Fig.1) as well.

Regarding Claim 8 (Updated)

HE'277 teaches using geometric programming with its advantageous ability to solve thousands of constraints (HE'277: Col.5 Lines 6-35). Further, HE'277 teaches these constraints can be displayed as tradeoff (implying at least two constraints with plurality of evaluated results) in form of curve representing target performance parameters range with two-dimensional range of plurality of performance points (HE'277: Col.6 Lines 3-24; Also see KR'527: Col.12 Line 63-Col.13 Line 23).

Regarding Claim 9 (Updated)

Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 10 (Updated)

Method claim 10 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 11 (Updated)

Method claim 11 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 13 (Updated)

Method claim 13 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 14 & 15 (Updated)

Method claims 14 & 15 disclose similar limitations as claim I and are rejected for the same reasons as claim 1.

Limitation disclosed as "design goals" is further disclosed as "performance parameter". HE'277 teaches producing a target model (HE'277: Col.4 Lines 61-67). Further, KR'527 teaches developing a device and product based on the target model (KR'527: Fig.6a, Col.9-I I Section Ill). The goals for device and product are interpreted as same goal, as indicated in the preamble "a product comprising a device" shows that product only has one device. Although "comprising" does not limited the scope, design goals can be seen in HE'277 (Col.6 Lines 1-24). KR'527 teaches target performance comprises plurality of performance points as points in the V/I curves (KR'527: Fig. 6c, Also see Fig.1 element 110). Further by applicant's disclosure, the tools to predict process and design variations are known in the art (Specification: [0033]).

Regarding Claim 16 (Updated)

Method claim 16 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 17 (Updated)

Method claim 17 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 18 (Updated)

Method claim 18 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 19 (Updated)

Method claim 19 discloses similar limitations as updated claim 1 and is rejected for the same reasons as claim 1.

KR'527 teaches developing a design for the device based on the target model (in simulator) (KR'527: Fig. 6a). KR'527 further teaches modifications to design wherein modification comprises modifying a particular feature and adding a particular feature of the design (KR'527: Col.6 Lines 34-59). KR'527 teaches determining primary parameters for a particular feature; determining secondary parameters from the said primary parameters (KR'527: at least in Col.2 Lines 51-63; also in Fig.6a-b-c- element 680-615-618; Col.13 Lines 10-23 — IN curve from L, T, N parameters).

KR'527: Col.2 Lines 5 1-63 states:

> Before an accurate model of semiconductor device 200 may be obtained, certain "parameters" must be extracted from semiconductor device 200, as illustrated in FIG. 1. Typically, a device simulator requires specific device "parameters" in order to provide a simulation. For example, one semiconductor device simulator requires five specific sets of parameters, as illustrated by parameters 103-107. Some of the parameters are extracted from device parameter extractor 102. Some of these parameters may correspond to physical measurements of transistor device 200, such as channel length L and doping concentration N+ I Primary parameters!, while other parameters may be based on or derived from these physical measurements or other parameters [secondary parameters].

KR'527 teaches determining secondary parameters from said primary parameters (KR'527: Fig.6a-b-c; Col.I3 Lines 10-23 — IN curve from L, T, N parameters) where the primary parameters are inputted into process simulator and secondary parameters are derived from primary parameters (element 680-615-618) and inputted into device simulator (Element 640).

KR'527 teaches balancing choices (KR'527: Col.2 Lines 20-24, Col.4 Lines 30-34) related to modification and particularly to primary and secondary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 — IN curve from L, T, N parameters; element 680-615-

618) so that target performance parameters will remain within first bound range and second bound range (KR'527: Abstract: Lines 19-27; Col.8 Lines 50-6 3).

Regarding Claim 20

KR'527 teaches correlating secondary parameters to at least one further secondary parameter (Col.2 Lines 51-63; Col.I2 Lines 8-62; Fig.6a-c & 7 a-c).

Regarding Claim 21

KR'527 teaches verifying that all primary and secondary parameters are within allowable limits (Col.13 Lines 24-62).

Regarding Claim 22

HE'277 teaches specifying parameters as first order and second order (HE'277: Col.II Line 59-Col.12 Line 15).

Regarding Claim 24

HE'277 teaches a method of developing a product (HE'277: Col.4 Lines 61-Col.5 Line 6) comprising a device with at least one performance attribute (HE'277: Col.3 Line 67 — Col.4 Line 5; Col.I Lines 10-15) wherein the said device comprises a integrated circuit component (HE'277: Col.6 Lines 58-62 — as transistor) and wherein said target model is create using performance parameter for the said performance attribute (HE'277: Col.5 Lines 40-46). The goals for device are based on the product — i.e. size of the transistors is dependent on the goal of the amplified in HE'277 (HE'277: Col.6 Lines 1-24). HE'277 teaches target performance parameter range includes a multiple first bounded range (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34; Also see ranges in KR'527 Fiq.1 Elements 103-107) and a second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 2 1-35). HE'277 teaches target performance parameter range comprises multiple first bounded range (due

to process variation being modeled as inequalities - HE'277 — single variation as function f0 and multiple variations as l~ - Col.7 Line 1-59 Col.20 Lines 6-21, Col.2I Lines 10-34; specially see Col.20 Lines 35-41) anda second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches each of said first bounded range~ comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.2I Lines 35-49) and; HE'277 teaches said second bounded range comprises performance parameters variations between designs for said design device (HE'277: Col.II Lines 40-Col. 12 Linel 6) as variations in at least the Length and Width of the transistor.

HE'277 teaches each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is contrainted by these curves.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process where the performance parameter are current voltage switch point, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided as V/I Curves (Abstract: Lines 19-

27; Col.8 Lines 50-63). The simulator simulates the computer model, created in the simulator, of the said product to determine if the product/device goals are met (KR'527: Fig.6a-6c).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes [nature of problem being solved] (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9- 55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, as is known in the art, numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to predictively examine possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 25 (Updated)

Method claim 25 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 26

Method claim 26 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 27

KR'527 teaches the step of accepting altered device design further comprises the steps of carrying out experiments on test chips (KR'527: Fig.3, actual to simulated data comparison & guard band generation Col.13 Lines 32-62).

Regarding Claim 30

KR'527 teaches calculating a primary parameter from a physical device feature as L, T and N values (KR'527: Col.1I at least in Lines 19-27); correlating a secondary parameter from said primary parameter as associating resulting IN curve with the L, T, N values (KR'527: Col.13 Lines 10-23); calculating secondary parameter based on the primary parameters based on predetermined primary to secondary correlation IN curve based on L, T, and N value equation (KR'527: Col. 13 Lines 10-23 Fig. 6c; HE'277 Equation 16) and comparing said secondary parameter to said target performance parameter (KR'527: Col.13 Lines 24-37).

Regarding Claim 31

KR'527 teaches correlating other secondary parameters from correlations to said secondary parameters as correlating the V/I curve to the various channel length and attributes (short, short long etc) (KR'527: Fig 5a, Element 500).

Regarding Claim 32

KR'527 teaches primary parameter is directly related to physical device feature as related to channel length, doping, gate oxide thickness (KR'527: Col.I I at least in Lines 19-27 & Table C).

Regarding Claim 33

KR'527 teaches correlating primary to secondary parameters (KR'527: Fig 5a, Element 500). Secondary parameters could be derived parameters like "beta" whose derivation using equation is well known in the art.

Regarding Claim 34

Method claim 34 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 35 (Updated)

Method claim 35 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 36 (Updated)

Product claim 36 discloses similar limitations as updated claim I and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product as alternate embodiment (HE'277: Col.22 Lines 1-21).

Regarding Claim 37 (Updated)

Product claim 37 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 38

Method claim 38 discloses similar limitations as claim 7 and is rejected for the same reasons as claim 7.

Regarding Claim 39

Method claim 39 discloses similar limitations as claim 8 and is rejected for the same reasons as claim 8.

Regarding Claim 40

Method claim 40 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product (storage device) readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method (HE'277: Col.22 Lines 1-21).

Regarding Claim 41 (New)

HE'277 teaches that multiple designs are directed to variations of a single design (HE'277: Col.I I Lines 40-Col.12 LineI6). For example changing the width (W) and lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.I, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 42 (New)

HE'277 teaches computer-implemented method (HE'277: Col.4 Lines 61-Col.5 Line 6) of developing a product comprising a device with at least one performance attribute

(HE'277: Col.6 Lines 1-24), wherein said device comprises an integrated circuit component (HE'277: Col.6 Lines 58-62 — a transistor), said method comprising: designing said product using a computer model that is based on a target model of said device, wherein said target model is created using said a target performance parameter range for said performance attribute (HE'277: Col.6 Lines 1- 24), wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range (HE'277: Col.5 Lines 27-35, 40-46; Also see ranges in KR'527 Fiq.1 Elements 103-107), wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point, wherein each of said multiple different designs is directed to a variation of a single design for said device (due to process variation being modeled as inequalities - HE'277 — single variation as function f0 and multiple variations as f~ - Col.7 Line I - 59; Col.20 Lines 6-21, Col.2I Lines 10-34; specially see Col.20 Lines 35-41, HE'277: Col.6 Lines 1-24), wherein said second bounded range is constrained is constrained (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48) by a most linear of said multiple model curves mad a least linear of said multiple model curves (Also See KR'527: Fig.I Element 110) and Wherein target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bound range around said least linear of said multiple model curves (Also See KR'527: Fig.1 Element 110).
Motivation to combine HE'277 with KR'527 is same as in claim I.

Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277 hereafter), in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission, further in view of U.S. Patent No. 6,028,994 issued to Peng et al (PE'994 hereafter).

Regarding Claim 28 & 29

Teaching of HE'277, KR'527 and applicant's own admission are shown in claim 24 rejections above.

HE'277 & KR'527 do not teach design goals for product, developing product fro from target model and product model simulation & alteration based on feedback.

PE'994 teaches teach design goals for product (PE'994: Col.2 Line 49-59 — predicted performance), developing product from target model as combined product & device model represented by product performance model (PPM) (PE'994: Fig. I; Col.6 Lines 57-67) and product model simulation & alteration based on feedback as self learning (PE'994: Fig.1 Step 64). The product is represented as package of wafer chip and the device is represented as wafer chip (PE'994: See Fig.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of PE'994 to HE'277 & KR'527. The motivation to combine would have been that HE'277 & KR'527 and PE'994 are attempting to design a model that can mimic and or predict the performance of the semiconductor model (PE'994: Abstract; HE'277 & KR'527: Abstracts) based on the input parameters. Further, teaches PE'994 specifying the input parameters as ranges (PE'994: Fig.3 Col.5 Lines 35-48) for performance which is very similar to the KR'527 teachings disclosed before relating to ranges for performance parameters.

2. Appellants' Position

a. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

Independent claims 1, 9, 14, 19, 24, 36, 40 and 42 stand rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. Specifically, the final rejection indicates that "Claims disclose generating computer model based on a target model where the target model is created using the performance parameters –the disclosure lacks enablement for creating such a computer model effectively based on

performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure." These rejections are traversed as explained below.

(1) Independent Claim 1

Claim 1 stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree based on the following discussion.

Paragraph [0023] of the specification indicates that different teams are involved in the design/manufacture of a final product. A device designer creates individual devices and the circuit designer utilizes the different devices to create a complete integrated circuit. However, problems can occur as device design progresses (see paragraph [0025]), which in turn can present a potential problem to circuit designers (see paragraph [0026]). Thus, the invention creates "a target model of the device" using target performance parameters for the device and device goals (see item 406 of Figure 4 and paragraph [0034]). "The circuit design process relies upon the target performance parameters 404 and target model 406 to create a circuit model 434 of the chip" (i.e., to create a computer model of the integrated circuit). This circuit model is then simulated in item 436 and the results of the simulation are checked to determine whether the circuit goals have been met (438) (see paragraph [0035]). Paragraph [0038] provides that this "inventive target-based compact model allows designers to evaluate variations in the process while maintaining the performance targets set out by the target model." Consequently, the Appellants submit that the process of generating a computer model for an integrated circuit based on a target model for a device where the target model is created using the performance parameters is enabled by the disclosure. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(2) Independent Claim 9

Claim 9 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(3) Independent Claim 14

Claim 14 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. Furthermore, since the rejection of claim 14 is based on a computer model and claim 14 is not limited by a computer model, this rejection is not warranted. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(4) Independent Claim 19

Claim 19 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. Furthermore, since the rejection of claim 19 is based on a computer model and claim 19 is not limited by a computer model, this rejection is not warranted. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(5) Independent Claim 24

Claim 24 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent

claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(6) Independent Claim 36

Claim 36 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. Furthermore, since the rejection of claim 36 is based on a computer model and claim 36 is not limited by a computer model, this rejection is not warranted. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(7) Independent Claim 40

Claim 40 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(8) Independent Claim 42

Claim 42 similarly stands rejected under 35 U.S.C. §112, first paragraph, as being based on a disclosure which is not enabling. The Appellants respectfully disagree for the same reasons set out above in paragraph VII.A.2.a.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

b. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Independent claims 1, 9, 14, 19, 24, 36, 40 and 42 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the final rejection provides that the claims disclose "limitation "first bound range" and "second bound range" for a "performance parameter". However, no specific ranges are provided by this claim thereby failing to provide for the metes and bound for the ranges." These rejections are traversed as explained below.

(1) Independent Claim 1

Claim 1 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on the following discussion.

Independent claim 1 as well as independent claims 9, 14, 19, 24, 36, 40 and 42 include the features of "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; and "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." While no specific ranges are provided in the claims, none are required. The range is application specific, as claimed. That is, each first bounded range is a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of the model curves for different designs for the device that achieve a same performance point. Similarly, the second range is constrained by at least two of these curves so as to comprise performance parameter variations between multiple different designs for the device.

Support for these ranges is found in paragraphs [0020]-[0030] of the published patent application and Figures 2-3. Paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed in terms of its permitted variability within a range constrained by at least two variables (i.e., within a target performance parameter range constrained by two variables): the first variable being variations in the manufacturing process and the second variable being variations in device design. Paragraph [0025] further explains that variations in the design of a device that still achieve the same performance point may result in different model curves (see model curves 20-22 of Figure 2 which represent multiple different designs for the same device that achieve the same performance point). That is, curves 20-22 were based on the same target model. Thus, as explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20 (i.e., it includes the second bounded range as claimed). Paragraphs [0029]-[0030] explain that this target performance parameter range is further expanded, based on processes windows, to include the first bounded ranges that are designated by dashed lines 25, 27 in Figure 2 which surround each of the design curves 20-22.

Specifically, as illustrated in Figures 2 and 3 and explained in paragraphs [0029]-[0030], the final target performance parameter range 30 includes all point between curves 20 and 22 (i.e., includes a second bounded range). It is further expanded to include all points between the upper edge of 27 of the processing window (i.e., the first bounded range) that is located around the most linear curve 22 and the lower edge 25 of the processing window (i.e., another first bounded range) that is located around the least linear curve 20 of the second bounded range). Thus, the final target performance parameter range also includes multiple first bounded ranges.

Again, no specific range is provided in the claims, nor is one required because for any given device the first bounded ranges will vary due to manufacturing process variations and the multiple model curves for different designs of the device that achieve a same performance point and the second bounded range will also vary based on the multiple model curves for the different designs of the device. That is, the ranges are

application specific, as claimed and as described in detail in the specification. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(2) Independent Claim 9

Claim 9 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(3) Independent Claim 14

Claim 14 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(4) Independent Claim 19

Claim 19 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(5) Independent Claim 24

Claim 24 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(6) Independent Claim 36

Claim 36 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(7) Independent Claim 40

Claim 40 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

(8) Independent Claim 42

Claim 42 similarly stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Appellants respectfully disagree based on

for the same reasons set out above in paragraph VII.A.2.b.(1), regarding independent claim 1. In view of the foregoing the Appellants respectfully request that the Board reconsider and withdraw this rejection.

c. REJECTIONS UNDER 35 U.S.C. §103 BASED ON HERSHENSON AND KRIVOKAPIC

Independent claims 1, 9, 14, 19, 24, 36, 40 and 42 stand rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. The Appellants respectfully traverse these rejections as discussed below.

The following is a summary of the cited prior art references:

Hershenson provides a system for providing automated synthesis of a globally optimal designs for a given circuit topology library. Specifically, referring to col. 5, line 35-col. 6, line 25, Hershenson provides that when a new semiconductor manufacturing process is initiated on the CAD system, models for the transistors (i.e., for a single component of an IC) are generated. The CAD system may include posynomial models of different levels of complexity that can be selected as needed based on the design requirements. The CAD system also includes a library of circuit topologies. Topologies are generally understood to be configurations (i.e., a relative arrangements of components, parts or elements (see Merriam-Webster Online Dictionary copyright © 2005 by Merriam-Webster, Incorporated). The library is divided into groups based on multi-component device type (e.g., op-amps, amplifiers for automatic gain control, limiters, oscillators, etc.). Thus, it is understood that the library includes, for each multi-component device, one or more different topologies or different relative arrangements of the individual components (e.g., transistors) within the devices.

After a transistor model is selected, a user selects a circuit topology or group of circuit topologies for the device from the library and then selects performance specifications for the desired device (i.e., for the desired circuit topology, such as an op-amp, oscillator, etc.). More specifically, for a given multi-component device (e.g., an

op-amp) the user determines the design parameters and performance specifications (see col. 10, line 35-col. 11, line 30). The system then generates a geometric program for the defined performance specification of the multi-component device, and based on a user-selected optimization mode, reformulates the geometric program as convex optimizations problems (see col. 7, lines 60-67). The program solves the geometric program for a globally optimal design of the integrated circuit topology for the user-defined defined specifications.

Krivokapic discloses a method for simulating the behavior of a mass-produced device. Specifically, Krivokapic recognizes that a designer must consider numerous transistor attributes in predicting semiconductor behavior and that a designer often must balance conflicting attributes to achieve a desired behavior (e.g. drain-to-source current vs. drain-to source voltage curves (I/V curve)). Various prior art device simulators model designed transistor behavior. However, prior art modeling do not accurately reflect mass-produced semiconductor device and do not use semiconductor manufacturing process simulations to generate distributions of manufactured semiconductor devices (see col. 3, line 66- col. 4, line 3). Thus, Krivokapic discloses an improved method for modeling designed transistor behavior in which I/V curves are obtained and used to show how choice of semiconductor device attributes, such as channel length, effect the guard band or manufacturability of such devices (see col. 4, lines 26-34). Specifically, referring to Figure 5 and the related text, performance values are obtained from devices with different attributes (step 500). A device simulator is calibrated based on the performance values (step 501). A process simulator is calibrated based on the performance values and the measured attributes of the devices (step 502). The process simulator is run (step 503). Then, the results of the process simulator are input into the device simulator to obtain I/V curves (step 504) and to determine the statistical worst-case I/V curves (step 505) by averaging the drain-to-source current values associated with drain to source voltage values. Parameters for device simulators are then extracted from the statistical worst-case I/V curves (step 506). The device simulator will output worst-case I/V curves in response to input parameters obtained from the statistical worst-case I/V curves (step

507) and finally, the worst case I/V curves can be compared to an ideal curve to obtain manufacturing guard bands (step 508).

The following is a summary of the present invention:

The present invention is concerned with creating a computer model for an integrated circuit using not only circuit goals for the integrated circuit itself, but also a target model for a device that will be incorporated into the integrated circuit. The target model for the device is created using a target performance parameter range for a given performance attribute of the device. This target performance range is further constrained by two variables (the device manufacturing process and device design). Specifically, the target performance parameter range comprises multiple first bounded ranges and a second bounded range. Each first bounded range represents a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of the device that achieve the same performance point. The second bounded range on the other hand is constrained by at least two of these multiple model curves (i.e., it comprises performance parameter variations between multiple different designs for the device.)

(1) Independent Claim 1

Independent claim 1 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that the cited prior art references do not teach or disclose the following claimed features of independent claim 1: (1) "wherein said target model is created using a target performance parameter range for said performance attribute and is adapted to predict process and design variations of said device;" (2) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (3) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (4) "wherein each of said multiple different designs is directed to a variation of a single

design for said integrated circuit"; and (5) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

The final rejection of claim 1 does not address the feature in claim 1 that the target model is *adapted to predict both process and design variations of said device.*

The final rejection further provides that both Hershenson and Krivokapic disclose "wherein said target model is create using performance parameter ranges for said performance attribute (HE'277: Col. 5 Lines 40-46; Also see ranges in KR'527 Fig. 1 Elements 103-107)." The final rejection further provides that Hershenson and Krivokapic both disclose "said target model is adapted to determine the said target performance parameter range of said device (HE'277:Col. 5 Lines 27-35; Col 6 Lines 1-48; Also See Kr'527-Fig. 1 element 109). The Appellants respectfully disagree.

Specifically, the claimed feature is "wherein said target model [for said device] is created using a target performance parameter range for said performance attribute [of said device]. It is not a target model that is created using performance parameter ranges for the performance attribute, nor is it a target model that is adapted to determine the target performance parameter range. Furthermore, the target model features cited in the Office Action as being disclosed by the prior art references are, by definition mutually exclusive. That is, the model can either be created using the range or it can determine the range, but not both (i.e., you can not determine the range with the model, if you actually need it in order to create the model). Also, even if for arguments sake, the Hershenson and Krivokapic both did teach a target model created using performance parameters ranges for a performance attribute, they do not go beyond that to teach the limiting feature in the present invention that the target model is created based on a single *target* performance parameter range for a given performance attribute as claimed.

Also, in Hershenson, a user selects a transistor model and a circuit topology from the CAD library and defines the performance specifications for a multi-component device (i.e., a circuit, such as an op-amp) (col. 5, lines 63-68). The system of Hershenson then generates a globally optimal design solution for achieving the defined performance

specifications (see col. 5, line 68-col. 6, line 25). Col. 5, lines 40-46 specifically provides that "When a new semiconductor manufacturing process is initialized on the CAD system of the present invention, models for the transistors in the process are generated. The system may include posynomial transistor models of different levels of complexity that can be selected as needed based on the design requirements." That is, the system of Hershenson may include multiple device models with different levels of complexity depending upon the design requirements. But Hershenson does not teach or disclose that a target model for a device (which is a component of an integrated circuit) is created using a target performance parameter range for a given performance attribute of that device, much less that such a target model is subsequently used to generate a computer model of the integrated circuit.

Similarly, the background of Krivokapic discusses that various device simulators have been built to model designed transistor behavior based upon specified transistor attributes (see col. 2, lines 33-38). Figure 1 of Krivokapic illustrates such a prior art method of modeling (to obtain I/V curves) (see col. 2, lines 39-42). Items 103-107 of Figure 1 refer to five specific sets of parameters required by one semiconductor device simulator (see col. 2, lines 55-59). The parameters 103-107 are extracted from a device parameter extractor and correspond to physical measurements or are derived from physical measurements of the transistor (see col. 2, lines 60-64). These five process parameters 103-107 are referred to as the five corners and illustrate the operational or behavioral envelope of typical manufactured device (col. 3, lines 32-35). Based on these measured and derived parameters, designers can model with a simulator, the worst-case IV curves and how the worst case transistors affect a circuit (see col. 3, lines 35-40). Thus, the cited portion of Krivokapic models the IV curve of a device using the overall operational/behavior envelope of a typical device (i.e., using actual measured parameters or parameters derived from measured parameters from the same type device manufactured under various different process conditions) (see col. 3, lines 5-40). It does not create a target model for a device (which is a component of an integrated circuit) using a target performance parameter range for a given performance attribute of that

device, much less that this target model is subsequently used to generate a computer model of the integrated circuit.

The Office Action further provides that Hershenson "teaches *target performance parameter range comprises multiple first bounded range* (due to process variation being modeled as inequalities –HE'277-single variation as function f_o and multiple variations as f_i-Col. 7, line 1-59; Col. 20 Lines 6-21, Col. 21 Lines 10-34; specially see Col. 20 Lines 35-41" *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device)-HE'277: Col. 5 Lines 40-48. The circuit topologies pointed out further for more complex elements e.g., (herein the product built from the device HE'277 Col. 5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col 6 Lines 21-35)." The Appellants respectfully disagree.

Specifically, the Appellants respectfully disagree with the finding that col. 7, line 1-59; col. 20, lines 6-21; col. 21, lines 10-3; and col. 20, lines 35-41, of Hershenson, teach the multiple first bounded ranges feature of the present invention. Hershenson at col. 7, lines 1-5, indicates the invention optimizes circuit design by modeling circuit operation using geometric programs and solving the geometric programs to provide optimal design parameter values. Col. 7, lines 5-59, describes generally that a geometric program is an optimization problem having a specified form without references to what variables are used in the equations or what they solved for. Col. 20, line 6-col. 21, line 67, discusses an additional embodiment of the invention where the method is for developing a circuit design that meets a set of specifications for a set of values of parameters rather than specifications for known or fixed parameters. The Appellants submit that *a set* of specifications for *a set* of values of parameters necessarily does not amount to the *multiple bounded first bounded ranges* included in the target performance parameter range of the claimed invention. Additionally, the referred to values of parameters (e.g., transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages, and load capacitances) correspond to

specifications for a circuit and not to the specifications for a device (e.g., a transistor) that is incorporated into the circuit, as in the present invention. That is, in the present invention, the target performance parameter range is used to create a target model for a device and then a computer model for a circuit that comprises the device is generated based on the target model. Whereas, in one of the method embodiments of Hershenson, a transistor model is selected from a library and the circuit topology is also selected (see col. 5, lines 63-65). Next, a set of specifications to meet a set of values of parameters for the circuit is selected (as opposed to specifications for known or fixed parameters of the circuit) and then the geometric program is generated (see col. 20, line 6-col. 21, line 68). Thus, Hershenson does not teach or suggest that the target model for a device within an integrated circuit is created using a target performance parameter range for a performance attribute of the device, much less that this target performance parameter range of the device's performance attribute comprises "multiple first bounded ranges".

The Appellants further disagree with finding that col. 5, lines 40-51 and col. 6, lines 21-35 of Hershenson teach the second bounded range feature of the present invention. As discussed above, col. 5, lines 40-48, of Hershenson provides that "When a new semiconductor manufacturing process is initialized on the CAD system of the present invention, models for the transistors in the process are generated. The system may include posynomial transistor models of different levels of complexity that can be selected as needed based on the design requirements." That is, the system of Hershenson may include multiple device models with different levels of complexity depending upon the design requirements. Col. 5, lines 50-51 of Hershenson provides that the CAD system can include a library of circuit topologies for a large number of devices. Col. 5, line 61-col. 6, line 36 provides that after a transistor model is selected from the library, a circuit topology or group of circuit topologies can be selected and further selects the performance specifications for the desired device (i.e., for the circuit itself not the transistor). The system of Hershenson generates a geometric program by selecting one of three optimization modes. The solution provided is a globally optimal solution for the defined circuit performance specifications. Thus, Hershenson does not teach or suggest

that the target model for a device (i.e., for a component of the integrated circuit) is created using a target performance parameter range for a performance attribute of the device, much less that the target performance parameter range of the device's performance attribute comprises both "multiple first bounded ranges" and "a second bound range".

The Office Action provides that Hershenson teaches "each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point (HE'277:Col. 20 Lines 6-21, Col. 21 Lines 10-60; Also See Col. 20 Lines 27-60; performance point Col. 21 Lines 35-49). The Appellants respectfully disagree.

As discussed above, Hershenson at col. 20, line 6-col. 21, line 67, discusses a method of developing circuit designs that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). Nothing in the cited portion of Hershenson indicates that each one of multiple first bounded ranges comprises "a range of performance parameter variations due to manufacturing process variations", much less that each one is "based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point."

The Office Action provides that Hershenson teaches "each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE '277: Col. 6 Lines 1-24). The second bounded range is constrained by these curves. The Appellants respectfully disagree.

As discussed previously, Hershenson at col. 5, lines 40-63, discloses a CAD library that stores transistor models, including but not limited to posynomial transistor models of different levels of complexity. Then, a user selects a transistor model (e.g., a posynomial transistor model) as needed based on the design requirements and after the transistor model is selected it is processed by the system. Specifically, col. 6, lines 1-24,

of Hershenson, discusses the fact that after selecting a transistor model, a circuit topology and circuit performance specifications, the system generates a geometric program for the defined performance specifications. Nothing in the cited portion of Hershenson teaches or discloses that the system uses multiple different designs for the device that are directed to a variation of a single design for the integrated circuit, rather as set out above only a single transistor model is selected and the integrated circuit design is optimized in light of that transistor model selection.

It is unclear what the Examiner is referring to by the statement "The second bounded range is constrained by these curves." Nothing in the cited portion of Hershenson (i.e., col. 6, lines 1-24) teaches or discloses multiple model curves, much less that a second bounded range of a target performance parameter range of a performance attribute of a device in an integrated circuit is constrained by "at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Therefore, independent claim 1 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 2-3 and 5-8 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(2) Independent Claim 9

Independent claim 9 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 9: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said

first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Furthermore, the Appellants submit that the cited prior art references do not teach the additional feature in independent claim 9 of "designing said product using a computer model that is based on a target model of said device, wherein said target model is created using a target performance parameter range for said performance attribute;" The final rejection of claim 9 does not address each of the claimed features but rather refers to the rejection of claim 1. However, claim 1 does not include a "designing" limitation and, thus, the rejection of claim 1 does not address the feature *designing said product* (which has a device comprising an integrated circuit component) using a computer model that is based on a target model of said device.

Therefore, independent claim 9 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 10-11 and 13 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(3) Independent Claim 14

Independent claim 14 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 14: (1) "wherein said target performance parameter range comprises

multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Furthermore, the Appellants submit that the cited prior art references do not teach the additional features in independent claim 14 of: (1) "developing device goals for said device, wherein said device goals are based on product goals;" (2) "producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device;" and (3) "designing said product with said device based on said target model."

First, the final rejection indicates that Hershenson teaches "producing a target model (HE'277:Col. 4 lines 61-67). The Appellants respectfully disagree. The cited portion of Hershenson only refers optimizing circuit designs generally by modeling circuit operations using polysnomial functions. It does not disclose developing a *target model*. Furthermore, the final rejection of independent claim 14 does not address at all the limiting feature in claim 14 of "wherein said target model is adapted to predict process and design variations of said device". As mentioned above, this feature was also not addressed in the final rejection of independent claim 1.

Additionally, the final rejection provides that Krivokapic "teaches developing a device and product based on the target model (KR'527:Fig.6A, Col.9-11 Section III). The goals for the product are interpreted as the same goal, as indicated in the preamble "a product comprising a device" show that the product only has one device. Although "comprising" does not limited the scope, design goals can be seen in HE'277 (Col. 6 Lines 1-24). The Appellants respectfully disagree.

Specifically, as discussed above, Krivokapic teaches a method of modeling the behavior of a mass-produced device (e.g., a transistor) to determine statistical worst case curves and predict the behavior of a device manufactured on a processing line. It does not teach developing a device and product based on a target model. Furthermore, the Appellants submit that the product and the device, as claimed, are separate and distinct patentable features as are the product goals and the device goals. The fact that the preamble refers to a "product comprising a device" does not limit the invention to a product having only one device. The subsequent claim language clearly indicates that the product and device are separate and distinct from each other in that the product, only after the target model for the device is produced, is designed with the device based on the target model. If the product and the device were interpreted as being the same thing, there would be no need to *design* the product after producing the target model for the device. Similarly, if the device goals and product goals were interpreted as the same goals, then there would be no need to *develop* device goals based on product goals.

Therefore, independent claim 14 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 15-18 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(4) Independent Claim 19

Independent claim 19 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 19: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to

manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Therefore, independent claim 19 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 20-22 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(5) Independent Claim 24

Independent claim 24 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 24: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

The Appellants also respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c.(3) with regard to independent claim 3, the cited prior art references

do not teach the additional features in independent claim 24 of "developing device goals for said device, wherein said device goals are based on product goals." Finally, the final rejection of claim 24, while addressing the feature of simulating based on a computer model, does not address the feature of "creating a computer model for said product, wherein said computer model of said product is based on said target model".

Therefore, independent claim 24 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 25-35 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(6) Independent Claim 36

Independent claim 36 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 36: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

The Appellants also respectfully submit that the cited prior art references do not teach the additional feature in independent claim 36 of "a set of subroutines created using a target performance parameter range for said performance attribute, wherein said set of

subroutines, when executed by said computer predict process and design variations of said device." This feature and, more particularly the idea a set of subroutines is executed to predict process and design variations of a device, is not addressed in the final rejection of the claim. Claim 36 was rejected for the same reasons as claim 1. As mentioned above, the final rejection of claim 1 does not address predicting *both process and design variations of said device*. The only other information provided in the final rejection of claim 36 relates to the fact that Hershenson which indicates that the invention of Hershenson can be implemented as a computer program product.

Therefore, independent claim 36 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claims 37-39 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections.

(7) Independent Claim 40

Independent claim 40 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 40: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

The Appellants also respectfully submit that, for the same reasons cited above (e.g., in paragraph VII.A.2.c (3) with regard to independent claim 14, in paragraph VII.A.2.c(5) with regard to claim 24 and in paragraph VII.A.2.c(6) with regared to claim 36), the cited prior art references do not teach the additional features in independent claim 36 of "producing a target model of a device for a product using a target performance parameter range for a performance attribute of said integrated circuit device, wherein said device comprises an integrated circuit component and wherein said target model comprises a set of subroutines that are adapted to predict process and design variations of said device" and "creating a computer model of said product, wherein said computer model of said product is based on said target model."

Therefore, independent claim 40 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. Furthermore, dependent claim 41 is similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejections

(8) Independent Claim 42

Independent claim 42 stands rejected under 35 U.S.C. §103 as being unpatentable over Hershenson in view of Krivokapic. Appellants respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c (1) with regard to independent claim 1, the cited prior art references do not teach or disclose the following claimed features of independent claim 40: (1) "wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range"; (2) "wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point"; (3) "wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit"; and (4) "wherein said second bounded range is

constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device."

Therefore, independent claim 40 is patentable over Hershenson in combination with Krivokapic and/or the Appellants' admissions. In view of the foregoing, the Board is respectfully requested to reconsider and withdraw the rejection.

d. CLAIM INTERPRETATION

The Appellants traverse the claim interpretation set out in paragraphs 8-11 of the final rejection.

Regarding the term "performance parameter", the Appellants submit that performance parameter and performance attribute, as defined in the specification, are not limited to a "current voltage switch-point" of a transistor computer model. Rather as discussed in paragraph [0017]-[0018], "the invention is also applicable to any component of any product, where the performance attributes of that component "help determine the functionality of the integrated product. Examples, include chemical components and subcomponents of drugs, or the insolue of a show, or the foam insulator of a hot tub. In each example, the former is the "device" and the latter is the "product"." The "manufacturing process can be developed to optimize certain "performance parameters" of the device. In our examples a "performance parameter" could be the current-voltage switchpoint of a transistor; solubility of a component of a drug; the rigidity of an insole; or the coefficient of thermal expansion of foam insulator for a hot tub." Thus, the term performance parameter is not limited specifically to the current voltage switchpoint of a transistor, it could be any other parameter of any other device that could be used to "help determine the functionality of the integrated product."

Regarding the phrase "second bounded range", according to the specification the second bounded range represents performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] and illustrated in Figures 2-3. Specifically, paragraph [0020] indicates that rather than specifying the performance parameter as a single target point, the parameter is expressed

in terms of its permitted variability within a range that is constrained by at least two variables (i.e., within a target performance parameter range that is constrained by two variables). The first variable being the manufacturing process and the second being variations in device design. Paragraph [0025] of the specification explains that variations in a design of a device, which still achieve the same performance point, may results in different model curves. These model curves are illustrated as curves 20-22 in Figure and represent multiple different designs for the same device. As explained in paragraph [0028], the target performance parameter range includes all points between the most linear curve 22 and the least linear curve 20. This reflects the second bounded range, as claimed.

Regarding the term "primary parameters", paragraph [0039] provides that "For the purposes of this application, "primary device parameters" are performance characteristics that are directly related to the specific physical feature. For example, in MOSFET designs, the overlap capacitance (Cov) is directly related to the length of the physical overlap of the gate material over the diffusion and extension (or lightly-doped drain) implants and the gate oxide thickness... Similarly, inversion capacitance (Cinv) is directly related to capacitive channel length).

Regarding the term "secondary parameters", paragraphs [0040]-[0041] provide that there is a correlation between primary and secondary parameters. Secondary parameters are calculated based on one or more primary parameters. The secondary parameters are constrained or derived as opposed to independent, etc.

e. CLAIM OBJECTIONS

The Amendment filed under 35 U.S.C. §1.116 included claim amendments designed to overcome the objections, which refer to typographical erros. However, the amendments were not entered. Thus, the Appellants anticipate filing an amendment under 37 C.F.R. §1.312 after allowance to ensure that the errors are corrected.

B. CONCLUSION

In view the forgoing, the Board is respectfully requested to reconsider and withdraw the rejections of claims 1-3, 5-11, 13-22, and 24-42. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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/Pamela M. Riley/
Pamela M. Riley, Esq.
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD, 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer No. 29154

IX. CLAIMS APPENDIX

1. A simulator comprising:

a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said computer model is generated based on a target model for said device and wherein said target model is created using a target performance parameter range for said performance attribute and is adapted to predict process and design variations of said device; and

a processor in communication with said memory and adapted to determine said target performance parameter range and to execute said computer model,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is directed to a variation of a single design for said integrated circuit, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device.

2. The simulator in claim 1, wherein said second bounded range is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves and wherein said target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

3. The simulator in claim 1, wherein said target performance parameter range is the same for a target model of said device and a final hardware design of said device.

4. (Cancelled).

5. The simulator in claim, wherein said target performance parameter range is bounded by said multiple first bounded ranges and said second bounded range.

6. The simulator in claim 1, wherein said multiple different designs of said device are permitted to vary as long as target performance parameters are maintained within said target performance parameter range.

7. The simulator in claim 1, wherein said target performance parameter range comprises a plurality of performance points.

8. The simulator in claim 1, wherein said target performance parameter range comprises at least a two-dimensional range of a plurality of performance points.

9. A computer-implemented method for designing a product having a device comprising an integrated circuit component, wherein said product is tolerant to variance in a given target performance parameter for a given performance attribute of said device, said method comprising:

designing said product using a computer model that is based on a target model of said device, wherein said target model is created using a target performance parameter range for said performance attribute,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is directed to a variation of a single design for said device, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device.

10. The method of claim 9, wherein said second bounded range is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves and wherein said target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

11. The method of claim 9, wherein said target performance parameter range is the same for a target model of said device and a final hardware design of said device.

12. (Cancelled).

13. The method in claim 9, wherein said multiple different designs of said device are permitted to vary within said model as long as said given target performance parameter remains within said target performance parameter range range.

14. A method of developing a product comprising a device with at least one performance attribute, wherein said device comprises an integrated circuit component, said method comprising:

developing device goals for said device, wherein said device goals are based on product goals;

developing a target performance parameter range for said performance attribute based on said device goals,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is direct to a variation of a single design for said device, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device;

producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device; and

designing said product with said device based on said target model.

15. The method of claim 14, wherein said target performance parameter range comprises a plurality of performance points.

16. The method of claim 14, wherein said second bounded range is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves and wherein said target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

17. The method of claim 14, wherein said target performance parameter range is the same for said target model of said device and a final hardware design of said device.

18. The method in claim 14, wherein said multiple different designs are permitted to vary as long as target performance parameters are maintained within said target performance parameter range.

19. A method of designing a device with at least one performance attribute, wherein said device comprises an integrated circuit component said method comprising:

providing a target model for said device;

wherein said target model is created based on a target performance parameter range for said performance attribute,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprise a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is direct to a variation of a single design for said device, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device;

developing a design for said device based on said target model;

proposing a modification of said design, wherein said modification comprises one of adding a particular feature into said design and modifying said particular feature already in said design;

determining primary parameters for said particular feature;

determining secondary parameters from said primary parameters; and

balancing design choices related to said modification and, particularly, to said primary parameters and said secondary parameters in order to maintain device performance within said said target performance parameter range.

20. The method of claim 19, wherein said step of determining secondary parameters further comprises the steps of:

determining at least one further secondary parameter from said secondary parameters; and

correlating said secondary parameters to said at least one further secondary parameter.

21. The method of claim 19, further comprising the step of verifying that all primary and secondary parameters are within allowable limits.

22. The method of claim 19, wherein said primary parameters comprise first-order primary parameters and second-order primary parameters.

23. (Cancelled).

24. A method of developing a product comprising a device with at least one performance attribute, wherein said device comprises an integrated circuit component said method comprising:

developing device goals for said device, wherein said device goals are based on product goals for said product;

developing a target performance parameter range for said performance attribute based on said device goals,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is direct to a variation of a single design for said device, and

wherein said second bounded range is constrained at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device;

producing a target model of said device based on said device goals and said target performance parameter range, wherein said target model is adapted to predict process and design variations of said device;

creating a computer model of said product, wherein said computer model of said product is based on said target model; and

simulating said computer model of said product to determine whether said product goals have been met.

25. The method of claim 24, further comprising:

altering a device design to produce an altered device design; and

accepting said altered device design only if said altered device design performs within said target performance parameter range.

26. The method of claim 25, further comprising:

refining said target model based on said altered device design; and

designing at least said product based on said refined target model.

27. The method of claim 25, wherein said step of accepting said altered device design further comprises the steps of carrying out experiments on test chips.

28. The method of claim 24, wherein said step of designing said product further comprises:

providing design goals for said product; and

developing a product model from said target model and from said design goals for said product.

29. The method of claim 28, further comprising:

simulating said product model;

determining whether said design goals for said product have been met; and

altering said design of said product if said product design goals have been met.

30. The method of claim 24, wherein said accepting process comprises:

calculating a primary parameter from a physical device feature;

calculating a secondary parameter based on said primary parameter; and

comparing said secondary parameter to said target performance parameter.

31. The method of claim 30, further comprising correlating other secondary parameters from correlations to said secondary parameters.

32. The method of claim 30, wherein said primary parameter is directly related to said physical device feature.

33. The method of claim 30, wherein said calculating of said secondary parameter is performed using predetermined primary-to-secondary correlation calculations.

34. The method of claim 24, wherein said target performance parameters are the same for a target model of said device and a final hardware design of said device.

35. The method of claim 24, wherein device design is permitted to vary as long as target performance parameters are maintained within said target performance parameter range.

36. A program storage device readable by computer and tangibly embodying a model of an integrated circuit device that has at least one performance attribute, said model, executable by said computer, comprising:

a set of subroutines created using a target performance parameter range for said performance attribute, wherein said set of subroutines, when executed by said computer,

predict process and design variations of said device,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded range comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is direct to a variation of a single design for said device, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device.

37. The program storage device in claim 36, wherein said second bounded range is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves and wherein said target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

38. The program storage device in claim 36, wherein said performance parameter comprises a plurality of performance points.

39. The program storage device, wherein said performance parameter comprises at least a two-dimensional range of a plurality of performance points.

40. A program storage device readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method, said method comprising:

producing a target model of a device for a product using a target performance parameter range for a performance attribute of said integrated circuit device, wherein said device comprises an integrated circuit component and wherein said target model comprises a set of subroutines that are adapted to predict process and design variations of said device,

wherein said target performance parameter range includes multiple first bounded ranges and a second bounded range,

wherein each of said first bounded range comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of for said device that achieve a same performance point,

wherein each of said multiple different designs is direct to a variation of a single design for said device, and

wherein said second bounded range is constrained by at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device; and

creating a computer model of said product, wherein said computer model of said product is based on said target model.

41. The method of claim 19, wherein said second bounded range is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves and wherein said target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

42. A computer-implemented method of developing a product comprising a device with at least one performance attribute, wherein said device comprises an integrated circuit component, said method comprising:

designing said product using a computer model that is based on a target model of said device, wherein said target model is created using said a target performance parameter range for said performance attribute,

wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,

wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point,

wherein each of said multiple different designs is directed to a variation of a single design for said device,

wherein said second bounded range is constrained is constrained by a most linear of said multiple model curves and a least linear of said multiple model curves, and

wherein target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bounded range around said least linear of said multiple model curves.

X. EVIDENCE APPENDIX

There is no other evidence known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There is no other related proceedings known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.